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# Claims

[c1] 1.A bipolar transistor comprising:
a patterned isolation region formed below an upper surface of a semiconductor substrate; and
a single crystal extrinsic base formed on an upper surface of said isolation region.

[c2] 2.The bipolar transistor of claim 1, wherein said single crystal extrinsic base comprises a portion of said semiconductor substrate located between said upper surface of the isolation region and said upper surface of the semiconductor substrate.

[c3] 3.The bipolar transistor of claim 1, further comprising a single crystal intrinsic base, wherein a portion of said single crystal extrinsic base merges with a portion of said single crystal intrinsic base.

[c4] 4.The bipolar transistor of claim 1, wherein said isolation region electrically isolates said single crystal extrinsic base from a collector.

[c5] 5.The bipolar transistor of claim 4, wherein said single crystal intrinsic and extrinsic bases separate said collector from an emitter.

[c6] 6.The bipolar transistor of claim 1, wherein said single crystal extrinsic base comprises epitaxially-grown silicon.

[c7] 7.The bipolar transistor of claim 1, wherein said isolation region comprises an insulator, and wherein said insulator comprises oxide.

[c8] 8.The bipolar transistor of claim 1, wherein said isolation region comprises any of a shallow trench isolation region and a deep trench isolation region.

[c9] 9.A bipolar transistor comprising:
a semiconductor substrate;
a sub-collector in said semiconductor substrate;
a collector adjacent said sub-collector;
a patterned isolation region encapsulated within said semiconductor substrate;
a single crystal extrinsic base over said isolation region; and
an emitter adjacent said single crystal extrinsic base.

[c10] 10.The bipolar transistor of claim 9, wherein said single crystal extrinsic base comprises a portion of the semiconductor substrate located between an upper surface of the isolation region and an upper surface of the semiconductor substrate.

[c11] 11.The bipolar transistor of claim 9, further comprising a single crystal intrinsic base, wherein a portion of said single crystal extrinsic base merges with a portion of said single crystal intrinsic base.

[c12] 12.The bipolar transistor of claim 9, wherein said isolation region electrically isolates said single crystal extrinsic base from said collector.

[c13] 13.The bipolar transistor of claim 12, wherein said single crystal intrinsic and extrinsic bases separate said collector from said emitter.

[c14] 14.The bipolar transistor of claim 9, wherein said single crystal extrinsic base comprises epitaxially-grown silicon.

[c15] 15.The bipolar transistor of claim 9, wherein said isolation region comprises an insulator, and wherein said insulator comprises oxide.

[c16] 16.The bipolar transistor of claim 9, wherein said isolation region comprises any of a shallow trench isolation region and a deep trench isolation region.

[c17] 17.A method of forming a bipolar transistor, said method comprising:
forming a patterend isolation region below an upper sur-

face of a semiconductor substrate; and
forming a single crystal extrinsic base on an upper surface of said isolation region.

[c18] 18.The method of claim 17, wherein said single crystal extrinsic base comprises a portion of the semiconductor substrate located between said upper surface of the isolation region and said upper surface of the semiconductor substrate.

[c19] 19.The method of claim 17, further comprising forming said single crystal intrinsic base over said semiconductor substrate, wherein a portion of said single crystal extrinsic base merges with a portion of said single crystal intrinsic base.

[c20] 20.The method of claim 17, wherein said isolation region electrically isolates said single crystal extrinsic base from a collector.

[c21] 21.The method of claim 20, wherein said single crystal intrinsic and extrinsic bases separate said collector from an emitter.

[c22] 22.The method of claim 17, wherein said single crystal extrinsic base comprises epitaxially-grown silicon.

[c23] 23.The method of claim 17, wherein said isolation region

comprises an insulator, and wherein said insulator comprises oxide.

[c24] 24.The method of claim 17, wherein said isolation region comprises any of a shallow trench isolation region and a deep trench isolation region.

[c25] 25.A method of manufacturing a bipolar transistor, said method comprising:
performing an oxygen implant to form a patterned isolation layer underneath a substrate surface;
forming a single crystalline intrinsic base over said substrate;
depositing insulator layers over said single crystalline intrinsic base;
selectively etching portions of said insulator layers to expose portions of said single crystalline intrinsic base; and
forming a single crystalline extrinsic base over exposed portions of said single crystalline intrinsic base.

[c26] 26.The method of claim 25, further comprising:
converting any polycrystalline portions and a portion of said single crystalline extrinsic base of said bipolar transistor into oxide by performing a high pressure oxidation process over said single crystalline extrinsic base;
removing excess portions of said oxide; and

forming an oxide isolation layer over said single crystalline extrinsic base by performing a second high pressure oxidation process over said single crystalline extrinsic base.

[c27] 27.The method of claim 26, wherein said insulator layers comprise a silicon nitride layer deposited over a silicon dioxide layer.

[c28] 28.The method of claim 27, further comprising:
removing remaining portions of said silicon nitride layer;
forming a pair of isolation spacers adjacent a sidewall of said single crystalline extrinsic base and said oxide isolation layer and over said silicon dioxide layer;
removing exposed portions of said silicon dioxide layer unprotected by said isolation spacers thereby exposing said single crystalline intrinsic base; and
defining an emitter region over said single crystalline intrinsic base.

[c29] 29.The method of claim 25, wherein said single crystalline extrinsic base comprises a portion of the substrate located between an upper surface of the patterned isolation layer and an upper surface of the substrate.

[c30] 30.The method of claim 25, wherein a portion of said single crystalline extrinsic base merges with a portion of

said single crystalline intrinsic base.